

1 CLAIMS:

2 1. A method of forming a semiconductor memory device
3 comprising:

4 forming a plurality of openings over a substrate;

5 forming second sidewall spacers comprising a first dielectric
6 material within each of the openings;

7 narrowing the openings by covering interiors of the second sidewall
8 spacers with a second dielectric material that is different from the first
9 dielectric material;

10 filling the openings with conductive material to form a contact in
11 electrical communication with a node on the substrate;

12 selectively removing substrate material to define a first set of
13 containers having first container sidewalls;

14 forming first sidewall spacers adjacent the first container sidewalls;
15 and

16 selectively removing remaining substrate material adjacent the first
17 sidewall spacers to define a second set of containers.

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19 2. The method of claim 1, further comprising forming capacitors
20 in the containers separated only by the spacers.

1 3. The method of claim 1, further comprising:

2 forming a first capacitor plate in each of the first and second
3 containers, the first capacitor plate comprising hemispherical polysilicon
4 in electrical communication with a respective node within respective
5 containers of the first and second containers, respective first capacitor
6 plates being insulated from one another by the first sidewall spacers;

7 forming a dielectric layer covering each respective first capacitor
8 plate; and

9 forming a second capacitor plate on the dielectric layer.

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11 4. The method of claim 1, wherein filling the openings with
12 conductive material comprises filling the openings with conductive
13 polysilicon.

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15 5. The method of claim 1, wherein forming second sidewall
16 spacers within each of the openings comprises:

17 depositing a dielectric layer comprising silicon nitride to form the
18 first dielectric material; and

19 anisotropically etching the dielectric layer to expose the node.

1 6. The method of claim 1, wherein narrowing the openings
2 comprises:

3 depositing a layer of the second dielectric material comprising
4 silicon dioxide; and

5 anisotropically etching the layer of second dielectric material to
6 expose the node.

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8 7. The method of claim 1, wherein selectively removing substrate
9 material to define a first set of containers having first container sidewalls
10 comprises:

11 plasma etching the substrate material to form a first set of
12 containers;

13 forming a dielectric layer in the first set of containers; and

14 anisotropically etching the dielectric layer to form sidewalls in the
15 first set of containers.

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17 8. The method of claim 1, wherein selectively removing
18 remaining substrate material adjacent the spacers to define a second set
19 of containers comprises wet etching the remaining substrate material
20 selectively with respect to the first and second sidewall spacers.

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22 9. The method of claim 1, wherein forming an opening
23 comprises forming a bit line contact opening.

1 10. A method of forming a semiconductor memory device
2 comprising:

3 forming a plurality of openings over a substrate, individual
4 openings having at least one sidewall;

5 covering the at least one sidewall of the plurality of openings with
6 a first insulating material;

7 etching the first insulating material to form second sidewall spacers;

8 narrowing the openings by covering interiors of the second sidewall
9 spacers with a second insulating material that is different from the first
10 insulating material;

11 forming electrically conductive material in the openings to provide
12 contacts;

13 selectively removing substrate material to define a first set of
14 containers having container sidewalls, wherein defining the first set of
15 containers includes selectively etching the first set of containers relative
16 to the sidewall spacers and the electrically conductive material of the
17 contacts;

18 forming first sidewall spacers adjacent the container sidewalls; and

19 selectively removing remaining substrate material adjacent the first
20 sidewall spacers to define a second set of containers.

1 11. The method of claim 10, further comprising forming
2 capacitors in the containers separated only by the spacers.

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4 12. The method of claim 10, further comprising:
5 forming a first capacitor plate in each of the first and second
6 containers, the first capacitor plate comprising hemispherical polysilicon
7 in electrical communication with a respective node within respective
8 containers of the first and second containers, respective first capacitor
9 plates being insulated from one another by the first sidewall spacers;

10 forming a dielectric layer covering each respective first capacitor
11 plate; and

12 forming a second capacitor plate on the dielectric layer.

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14 13. The method of claim 10, wherein forming electrically
15 conductive material in the openings comprises filling the openings with
16 conductive polysilicon.

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18 14. The method of claim 10, wherein forming second sidewall
19 spacers within each of the openings comprises:

20 depositing a dielectric layer comprising silicon nitride to form the
21 first insulating material; and

22 anisotropically etching the dielectric layer to expose the node.

1 15. The method of claim 10, wherein narrowing the openings
2 comprises:

3 depositing a layer of the second insulating material comprising
4 silicon dioxide; and

5 anisotropically etching the layer of second insulating material to
6 expose the node.

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8 16. The method of claim 10, wherein selectively removing
9 substrate material to define a first set of containers having first container
10 sidewalls comprises:

11 plasma etching the substrate material to form a first set of
12 containers;

13 forming a dielectric layer in the first set of containers; and

14 anisotropically etching the dielectric layer to form sidewalls in the
15 first set of containers.

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17 17. The method of claim 10, wherein selectively removing
18 remaining substrate material adjacent the spacers to define a second set
19 of containers comprises wet etching the remaining substrate material
20 selectively with respect to the first and second sidewall spacers.

1 18. The method of claim 10, wherein forming a plurality of
2 openings over a substrate includes forming a plurality of bit line contact
3 openings over a substrate.

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5 19. A method of forming a contact comprising:
6 forming a sacrificial layer over a node on a substrate;
7 forming an opening through the sacrificial layer and extending to
8 the node;
9 forming a first dielectric sidewall coating an interior sidewall of the
10 opening;
11 forming a second dielectric sidewall coating an interior sidewall of
12 the first dielectric sidewall; and
13 forming a conductive plug within an interior sidewall of the second
14 dielectric layer and extending through the opening to the node.

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16 20. The method of claim 19, wherein forming a first dielectric
17 sidewall comprises:

18 depositing a layer of first dielectric material comprising silicon
19 nitride; and
20 anisotropically etching the layer of first dielectric material to
21 expose the node.

1 21. The method of claim 19, wherein forming a second dielectric
2 sidewall comprises:

3 depositing a layer of second dielectric material comprising silicon
4 dioxide; and

5 anisotropically etching the layer of second dielectric material to
6 expose the node.

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8 22. The method of claim 19, wherein forming a conductive plug
9 comprises forming a plug of conductive polysilicon in electrical
10 communication with the node.

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12 23. The method of claim 19, wherein forming a second dielectric
13 sidewall comprises forming a second dielectric sidewall that is thicker
14 than a thickness of the first dielectric sidewall.

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16 24. The method of claim 19, wherein forming a second dielectric
17 sidewall comprises forming a second dielectric sidewall that has a relative
18 dielectric constant that is less than a relative dielectric constant of the
19 first dielectric sidewall.

1 25. A method of forming a semiconductor memory device
2 comprising:

3 forming a plurality of openings over a substrate;
4 forming second sidewall spacers comprising a first dielectric
5 material within each of the openings;

6 filling the openings with conductive material to form a contact in
7 electrical communication with a node on the substrate;

8 forming a negative photoresist mask to define a first set of
9 openings;

10 etching substrate material through the first set of openings to
11 define a first set of containers having first container sidewalls;

12 forming first sidewall spacers adjacent the first container sidewalls;
13 and

14 selectively removing remaining substrate material adjacent the first
15 sidewall spacers to define a second set of containers.

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17 26. The method of claim 25, further comprising:

18 narrowing the openings by covering interiors of the second sidewall
19 spacers with a second dielectric material that is different from the first
20 dielectric material prior to filling the openings; and

21 forming capacitors in the containers separated only by the spacers.

1 27. The method of claim 25, further comprising:
2 forming a first capacitor plate in each of the first and second
3 containers, the first capacitor plate comprising hemispherical polysilicon
4 in electrical communication with a respective node within respective
5 containers of the first and second containers, respective first capacitor
6 plates being insulated from one another by the first sidewall spacers;
7 forming a dielectric layer covering each respective first capacitor
8 plate; and
9 forming a second capacitor plate on the dielectric layer.

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11 28. The method of claim 25, wherein filling the openings with
12 conductive material comprises filling the openings with conductive
13 polysilicon.

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15 29. The method of claim 25, wherein forming second sidewall
16 spacers within each of the openings comprises:
17 depositing a dielectric layer comprising silicon nitride to form the
18 first dielectric material; and
19 anisotropically etching the dielectric layer to expose the node.

1 30. The method of claim 25, wherein narrowing the openings
2 comprises:

3 depositing a layer of the second dielectric material comprising
4 silicon dioxide; and

5 anisotropically etching the layer of second dielectric material to
6 expose the node.

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8 31. The method of claim 25, wherein selectively removing
9 substrate material to define a first set of containers having first container
10 sidewalls comprises:

11 plasma etching the substrate material to form a first set of
12 containers;

13 forming a dielectric layer in the first set of containers; and

14 anisotropically etching the dielectric layer to form sidewalls in the
15 first set of containers.

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17 32. The method of claim 25, wherein selectively removing
18 remaining substrate material adjacent the spacers to define a second set
19 of containers comprises wet etching the remaining substrate material
20 selectively with respect to the first and second sidewall spacers.

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22 33. The method of claim 25, wherein forming an opening
23 comprises forming a bit line contact opening.

1 34. A bit line contact comprising:

2 a layer formed on a substrate and including an opening extending

3 through the layer to a node on the substrate;

4 a first dielectric sidewall formed in the opening and coating an

5 interior sidewall of the opening;

6 a second dielectric sidewall formed in the opening and coating an

7 interior sidewall of the first dielectric layer; and

8 a conductive plug formed within an interior sidewall of the second

9 dielectric layer and extending through the opening to the node.

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11 35. The bit line contact of claim 34, wherein the first dielectric

12 sidewall is formed of a first material and the second dielectric sidewall

13 is formed of a second material having a lower relative dielectric constant

14 than the first dielectric sidewall.

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16 36. The bit line contact of claim 34, wherein the conductive plug

17 comprises doped polysilicon.

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19 37. The bit line contact of claim 34, wherein the contact is

20 laterally surrounded by six capacitors.

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22 38. The bit line contact of claim 34, wherein the first dielectric

23 sidewall has an aspect ratio of twenty five or more.

1 39. The bit line contact of claim 34, wherein the first dielectric
2 sidewall comprises silicon nitride.

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4 40. The bit line contact of claim 34, wherein the second
5 dielectric sidewall comprises silicon dioxide.

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7 41. The bit line contact of claim 34, wherein the second
8 dielectric sidewall is thicker than the first dielectric sidewall.

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